SEMESTER S8

MIXED-SIGNAL VLSI DESIGN

Course Code	**PEEVT 865**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	5/3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT601 Analog VLSI Design, PCEVT50 Digital CMOS Design	**Course Type**	5 Credit Elective

Course Objectives:

1. To provide students with a comprehensive understanding of CMOS amplifier design, including small-signal modelling, frequency response analysis, and the implementation of various amplifier configurations such as common source, cascode, and folded cascode amplifiers.
2. To equip students with the skills to design and analyze CMOS differential amplifiers, including the use of current mirrors and techniques to enhance common-mode rejection ratio (CMRR), and to understand their application in high-performance circuits.
3. To familiarize students with the design and optimization of two-stage operational amplifiers, focusing on frequency compensation techniques like Miller compensation, and the development of stable bandgap references for reliable operation.
4. To teach the principles of data converter design, including DAC and ADC architectures, and to enable them to understand and implement various data conversion techniques such as resistor string, R-2R ladder, and different ADC types.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**CMOS Amplifiers** **MOS small signal model:** **CMOS Amplifiers**: Common source amplifier with resistive and active loads, Common source amplifier with source degeneration, Common gate and Common drain amplifier (only voltage gain and input and output	**9**

	impedances of the circuits), Frequency Response of CMOS Amplifiers **Cascode Amplifier:** Cascoded amplifier with cascade loads Folded cascode Amplifier.	
2	**CMOS Differential Amplifiers** **MOS Current Mirror:** Basic circuit, PMOS and NMOS current mirrors Simple and Cascode current mirror circuits. **CMOS Differential Amplifier:** Differential Amplifier with resistive, current source and current mirror loads, MOS telescopic cascode amplifier (only voltage gain and input and output impedance of the circuits) **Common-Mode Rejection Ratio (CMRR) and its Enhancement:** methods to measure and improve CMRR, and techniques such as common-mode feedback to enhance performance in noisy environments	**9**
3	**CMOS Operational Amplifier** **Two Stage Operational Amplifiers** Frequency compensation of OPAMPS Miller compensation**.** **Band gap References-** Supply Independent Biasing, Temperature independent references –band gap reference	**9**
4	**Data Converters:** DAC specifications, ADC specifications **DAC Architecture -** Resistor String, R-2R Ladder Networks, Current Steering, Charge Scaling, cyclic and Pipeline types. **ADC Architecture-** Flash type, The Successive approximation type and oversampling ADCs.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students select recent publications on a specific topic related to the course (eg. Differential Amplifier Design).
- Preparation of a report summarizing the findings, discussing the significance, and proposing future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and significant research papers.
- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured report with clear arguments.
- Originality (2 Marks): Innovative insights or perspectives.

3. Design Exercise (10 Marks)

Design a CMOS differential amplifier meeting specific requirements such as gain, input impedance, and common-mode rejection ratio (CMRR). Present the design through a schematic diagram and perform calculations to verify that the design meets the given specifications.

Criteria for Assessment:

1. **Design Accuracy (4 marks)**
    - Correct implementation of the differential amplifier design.
    - Accuracy in meeting the specified design parameters, such as gain, impedance, and CMRR.
2. **Calculation and Analysis (3 marks)**
    - Correctness and thoroughness of calculations related to amplifier performance.

- Proper analysis and justification of design choices.

3. **Schematic Presentation (2 marks)**
   - Clarity and correctness of the schematic diagram.
   - Proper labelling and organization of the components in the schematic.
4. **Design Justification (1 mark)**
   - Clear explanation of design choices and how they address the problem requirements.
   - Insight into the trade-offs made during the design process.

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Design and analyse various CMOS amplifiers, including common source, common gate, and common drain amplifiers, as well as cascode and folded cascode amplifiers, with an understanding of their frequency response and small-signal models.	**K3**
CO2	Implement and evaluate CMOS differential amplifiers with various loads, apply MOS current mirrors, and enhance common-mode rejection ratio (CMRR) using techniques such as common-mode feedback in noisy environments.	**K3**
CO3	Design and optimize two-stage operational amplifiers, apply frequency compensation techniques including Miller compensation, and develop bandgap references for stable supply-independent and temperature-independent biasing.	**K3**
CO4	Analyse and design data converters, including DACs and ADCs, by understanding their specifications, architectures, and various types such as resistor string, R-2R ladder, current steering, flash, successive approximation, and oversampling ADCs.	**K4**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO2	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO3	**2**	**3**	**2**	**2**	**3**	**1**	**1**		**1**			
CO4	**2**	**3**	**2**	**3**	**2**	**1**	**1**		**1**			

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	2000
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc22_ee37/preview
2	https://archive.nptel.ac.in/courses/117/101/117101106/
3	https://onlinecourses.nptel.ac.in/noc22_ee27/preview
4	https://nptel.ac.in/courses/117106034